WHAT IS CLAIMED IS:

1. An digital circuit having at least first and second edge-triggered devices, respectively receiving first and second clock signals, and a selectable circuit path for forming at least one scan path that includes the first and second edge-triggered devices, including:

a latch in the scan data path, the latch having a data input coupled to receive an output from the first device and an output coupled to an input of the second device, the latch being clocked by the second clock signal to temporarily hold data while the first and second devices change state.

2. The digital circuit of claim 1, including multiplexer circuits for selectively forming the scan data path in response to a test signal.

3. the digital circuit of claim 2, wherein the first and second devices form functional circuits in absence of the test signal.

4. The digital circuit of claim 1, wherein the first and second clock signals are asynchronous to one another.

5. A digital circuit structured to be subjected to scan testing, comprising,

a scan data input;

a scan data output;

at least first and second clock domains each including one or more edge-triggered devices, each clock domain receiving first and second clock signals;

a data path selectable in response to a test signal for form a scan data path between the scan data input and the scan data output that includes the first and second with a scan data path portion from an output of the first device to an input of the second device; and

a latch in the scan data path portion that is clocked by the second clock signal.

6. A method of scan-testing digital logic comprising at least first and second digital circuits having a data path from one to the other and respectively clocked

by first and second clock signals, each digital circuit including at least one edge-triggered device, the method including the steps of:

providing a latch element in the data path clocked by a test clock;

asserting a test signal to cause at least one serial scan chain to be formed that includes the first and second digital circuits;

operating the first, second, and test clock signals to cause the scan chain to receive test data such that the test clock assumes one state to hold the latch element while the edge-triggered devices are caused to change state by the first and second clock signals and the test clock then assumes a second state to allow data to pass along the test path from the one digital circuit to the other.